

<b>Notice of References Cited</b>	Application/Control No. 09/804,504		Applicant(s)/Patent Under Reexamination STEWART ET AL.	
	Examiner Thomas H. Stevens		Art Unit 2123	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-5,659,716	08-1997	Selvidge et al.	703/23
	C	US-5,548,794	08-1996	Yishay et al.	710/51
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	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

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	N	WO 94/06210	03-1994	PCT		703
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Babb et al., ("Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation" (MIT 1993)) 1993. pg.1-102
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.